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Electron Devices Meeting, 1991. Technical Digest., International , 8-11 Dec. 1991

Page(s): 295 -298

[\[Abstract\]](#) [\[PDF Full-Text \(340 KB\)\]](#) **IEEE CNF****2 NOR virtual ground (NVG)-a new scaling concept for very high density flash EEPROM and its implementation in a 0.5 um process***Bergemont, A.; Haggag, H.; Anderson, L.; Shacham, E.; Wolstenholme, G.;*

Electron Devices Meeting, 1993. Technical Digest., International , 5-8 Dec. 1993

Page(s): 15 -18

[\[Abstract\]](#) [\[PDF Full-Text \(308 KB\)\]](#) **IEEE CNF****3 High speed sub-halfmicron flash memory technology with simple stacked gate structure cell***Mori, S.; Sakagami, E.; Yamaguchi, Y.; Kamiya, E.; Tanimoto, M.; Tsunoda, H.; Hisatomi, K.; Egawa, H.; Arai, N.; Hiura, Y.; Yoshikawa, K.; Hashimoto, K.;*

VLSI Technology, 1994. Digest of Technical Papers. 1994 Symposium on , 7-9 June 1994

Page(s): 53 -54

[\[Abstract\]](#) [\[PDF Full-Text \(188 KB\)\]](#) **IEEE CNF**

---

**4 Flash-the memory technology of the future that's here today**

*Wett, T.; Levy, S.;*

Aerospace and Electronics Conference, 1995. NAECON 1995.,  
Proceedings of the IEEE 1995 National , Volume: 1 , 22-26 May 1995  
Page(s): 359 -364 vol.1

[\[Abstract\]](#) [\[PDF Full-Text \(420 KB\)\]](#) **IEEE CNF**

---

**5 Non-uniform current flow through thin oxide after  
Fowler-Nordheim current stress**

*Yamada, S.; Amemiya, K.; Yamane, T.; Hazama, H.; Hashimoto, K.;*  
Reliability Physics Symposium, 1996. 34th Annual Proceedings., IEEE  
International , 30 April-2 May 1996  
Page(s): 108 -112

[\[Abstract\]](#) [\[PDF Full-Text \(408 KB\)\]](#) **IEEE CNF**

---

**6 A 32-bit RISC microcontroller with 448K bytes of embedded  
flash memory**

*Kuo, C.; Chrudimsky, D.; Jew, T.; Gallun, C.; Choy, J.; Wang, B.;*  
*Pessoney, S.; Choe, H.; Harrington, C.; Eguchi, R.; Strauss, T.;*  
*Prinz, E.; Swift, C.;*  
Nonvolatile Memory Technology Conference, 1998. 1998  
Proceedings. Seventh Biennial IEEE , 22-24 June 1998  
Page(s): 28 -33

[\[Abstract\]](#) [\[PDF Full-Text \(644 KB\)\]](#) **IEEE CNF**

---

**7 Analog sense amplifiers for high density NOR flash  
memories**

*Pasotti, M.; Rolandi, P.L.; Canegallo, R.; Gerna, D.; Guaitini, G.;*  
*Lhermet, F.; Kramer, A.;*  
Custom Integrated Circuits, 1999. Proceedings of the IEEE 1999,  
16-19 May 1999  
Page(s): 247 -250

[\[Abstract\]](#) [\[PDF Full-Text \(372 KB\)\]](#) **IEEE CNF**

---

**8 A sampling weak-program method to tighten  
Vth-distribution of 0.5 V for low-voltage flash memories**

*Shiga, H.; Tanzawa, T.; Umezawa, A.; Taura, T.; Miyaba, T.; Saito,*

M.; Kitamura, S.; Mori, S.; Atsumi, S.;

VLSI Circuits, 1999. Digest of Technical Papers. 1999 Symposium on , 17-19 June 1999

Page(s): 33 -36

[\[Abstract\]](#) [\[PDF Full-Text \(232 KB\)\]](#) **IEEE CNF**

---

**9 Novel Bi-directional tunneling program/erase NOR (BiNOR) type flash EEPROM**

Yang, E.C.-S.; Cheng-Jye Liu; Tien-Sheng Chao; Ming-Chi Liaw; Hsu, C.C.-H.;

VLSI Technology, Systems, and Applications, 1999. International Symposium on , 8-10 June 1999

Page(s): 207 -210

[\[Abstract\]](#) [\[PDF Full-Text \(304 KB\)\]](#) **IEEE CNF**

---

**10 A new self-convergent programming and erase tightening by substrate-hot-electron injection for ETOX cells in triple-well**

Min-Hwa Chi; Chih-Ming Chen; Chih-Wei Hung; Yu-Hsiung Wang;

VLSI Technology, Systems, and Applications, 1999. International Symposium on , 8-10 June 1999

Page(s): 199 -202

[\[Abstract\]](#) [\[PDF Full-Text \(280 KB\)\]](#) **IEEE CNF**

---

**11 A channel-erasing 1.8 V-only 32 Mb NOR flash EEPROM with a bit-line direct-sensing scheme**

Atsumi, S.; Umezawa, A.; Tanzawa, T.; Taura, T.; Shiga, H.; Takano, Y.; Miyaba, T.; Matsui, M.; Watanabe, H.; Isobe, K.; Kitamura, S.; Yamada, S.; Saito, M.; Mori, S.; Watanabe, T.;

Solid-State Circuits Conference, 2000. Digest of Technical Papers.

ISSCC. 2000 IEEE International , 7-9 Feb. 2000

Page(s): 276 -277, 464-5

[\[Abstract\]](#) [\[PDF Full-Text \(325 KB\)\]](#) **IEEE CNF**

---

**12 A flash EEPROM cell with self-aligned trench transistor and isolation structure**

Nakagawa, K.; Yoshida, K.; Masuda, S.; Yoshino, A.; Sakai, I.;

VLSI Technology, 2000. Digest of Technical Papers. 2000 Symposium on , 13-15 June 2000

Page(s): 124 -125

[\[Abstract\]](#) [\[PDF Full-Text \(196 KB\)\]](#) **IEEE CNF**

---

**13 A flash IC card with programmable security code**

*Liu Kai; Pan li-yang; Zhu jun;*

ASIC, 2001. Proceedings. 4th International Conference on , 23-25

Oct. 2001

Page(s): 584 -587

[\[Abstract\]](#) [\[PDF Full-Text \(314 KB\)\]](#) **IEEE CNF**

---

**14 Influence of plasma edge damage on erase characteristics of NOR flash EEPROM using channel erase method**

*Dong-Kyu Lee; Lee, W.H.; Young-Ho Na; Keon-Soo Kim; Kun-Ok*

*Ahn; Kang-Deog Suh; Yonghan Roh;*

Reliability Physics Symposium Proceedings, 2002. 40th Annual , 7-11

April 2002

Page(s): 354 -358

[\[Abstract\]](#) [\[PDF Full-Text \(386 KB\)\]](#) **IEEE CNF**

---

**15 Novel ELFIN (embedded-metal-layer process for fully integrated NOR) cell for 16/64 Mbit flash EEPROM**

*Kawazu, Y.; Kayashi, T.; Ohno, M.; Ono, T.; Uchiyama, A.;*

Electronics Letters , Volume: 30 Issue: 15 , 21 July 1994

Page(s): 1209 -1210

[\[Abstract\]](#) [\[PDF Full-Text \(172 KB\)\]](#) **IEE JNL**

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Electron Devices, IEEE Transactions on, Volume: 50 Issue: 10, Oct. 2003

Page(s): 2104 -2111

[\[Abstract\]](#) [\[PDF Full-Text \(554 KB\)\]](#) **IEEE JNL****17 A self-convergence erase for NOR flash EEPROM using avalanche hot carrier injection***Yamada, S.; Yamane, T.; Amemiya, K.; Naruke, K.;*

Electron Devices, IEEE Transactions on, Volume: 43 Issue: 11, Nov. 1996

Page(s): 1937 -1941

[\[Abstract\]](#) [\[PDF Full-Text \(472 KB\)\]](#) **IEEE JNL****18 A multilevel approach toward quadrupling the density of flash memory***Kencke, D.L.; Richart, R.; Shyam Garg; Banerjee, S.K.;*

Electron Device Letters, IEEE, Volume: 19 Issue: 3, March 1998

Page(s): 86 -88

[\[Abstract\]](#) [\[PDF Full-Text \(108 KB\)\]](#) **IEEE JNL**

**19 Novel bi-directional tunneling program/erase NOR (BiNOR)-type flash EEPROM**

*Evans Ching-Song-Yang; Cheng-Jye Liu; Ming-Chi Liaw; Tien-Sheng Chao; Ching-Hsiang Hsu, C.;*

Electron Devices, IEEE Transactions on , Volume: 46 Issue: 6 , June

1999

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[\[Abstract\]](#) [\[PDF Full-Text \(184 KB\)\]](#) **IEEE JNL**

---

**20 A channel-erasing 1.8-V-only 32-Mb NOR flash EEPROM with a bitline direct sensing scheme**

*Atsumi, S.; Umezawa, A.; Tanzawa, T.; Taura, T.; Shiga, H.; Takano, Y.; Miyaba, T.; Matsui, M.; Watanabe, H.; Isobe, K.; Kitamura, S.; Yamada, S.; Saito, M.; Mori, S.; Watanabe, T.;*

Solid-State Circuits, IEEE Journal of , Volume: 35 Issue: 11 , Nov.

2000

Page(s): 1648 -1654

[\[Abstract\]](#) [\[PDF Full-Text \(152 KB\)\]](#) **IEEE JNL**

---

**21 Bandwidth optimization of flash memories with the RGP technique**

*Versari, R.; Esseni, D.; Falavigna, G.; Lanzoni, M.; Ricco, B.;*

Electron Devices, IEEE Transactions on , Volume: 48 Issue: 8 , Aug.

2001

Page(s): 1737 -1740

[\[Abstract\]](#) [\[PDF Full-Text \(128 KB\)\]](#) **IEEE JNL**

---

**22 Mobile ion-induced data retention failure in NOR flash memory cell**

*Lee, W.H.; Dong-Kyu Lee; Keon-Soo Kim; Kun-Ok Ahn; Kang-Deog Suh;*

Device and Materials Reliability, IEEE Transactions on , Volume: 1

Issue: 2 , June 2001

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[\[Abstract\]](#) [\[PDF Full-Text \(152 KB\)\]](#) **IEEE JNL**

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